III. Amendments to the Claims

Claims 1-38 are currently pending. Claims 24-38 have been withdrawn from consideration. Please cancel Claims 24-38. Please amend Claim 14 as set forth below. Please also add new Claims 39-52. This listing of claims replaces all prior versions and listing of the claims.

1. (original) A method of forming a one-transistor memory cell, comprising:

(a) forming a dielectric layer over a substrate having a pass-gate formed thereon;

(b) forming an opening in the dielectric layer to expose a portion of the substrate at least adjacent to the pass-gate;

(c) forming a capacitor dielectric layer on sidewalls of the opening in the dielectric layer and on the exposed portion of the substrate; and

(d) forming an electrode layer over the capacitor dielectric layer.

2. (original) The method of claim 1, wherein step (b) further comprises the steps of forming a recess in an isolation region within the substrate, and steps (c) and (d) further comprise forming the capacitor dielectric layer and the electrode layer within the recess of the isolation region.

3. (original) The method of claim 1, wherein steps (c) and (d) comprise:

after step (b), substantially conformally forming the capacitor dielectric layer over the dielectric layer;

forming a planarization layer over the electrode layer; and removing portions of the planarization layer, the capacitor dielectric layer and the electrode layer directly over the dielectric layer.

4. (original) The method of claim 3, wherein the planarization layer is a dielectric layer.

5. (original) The method of claim 3, wherein the planarization layer is a photoresist layer.

6. (original) The method of claim 5, further comprising the step of removing the photoresist layer within the opening of the dielectric layer after the removing portions step.

7. (original) The method of claim 1, wherein step (b) further comprises using a second dielectric layer formed on a sidewall of the pass-gate as an etching stop layer.

8. (original) The method of claim 1, wherein a space between the pass-gate and the exposed portion of the substrate is from about 400Å to about 1500Å.

9. (original) The method of claim 1, wherein the capacitor dielectric layer comprises a high dielectric constant material layer.

10. (original) The method of claim 9, wherein the capacitor dielectric layer is formed by atomic layer deposition (ALD).

11. (original) The method of claim 9, wherein the electrode layer comprises a metal layer.

12. (original) The method of claim 1 further comprising:

(e) forming a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

(f) forming a doped region within the substrate and adjacent to the pass-gate and the electrode layer.

13. (original) The method of claim 12, wherein the doped region has a dopant concentration lower than that of the S/D region.

14. (currently amended) A method of forming a one-transistor memory cell, comprising:

(a) forming an isolation region within a substrate, a pass-gate over the substrate and a first dielectric layer over the substrate including over the isolation region and the pass-gate;

(b) forming an opening through the first dielectric layer to expose a portion of the substrate at least adjacent to the pass-gate, wherein a second dielectric layer on a sidewall of the pass-gate is used as an etch stop layer, and a recess within the isolation region;

(c) forming a capacitor dielectric layer on sidewalls of the opening in the first dielectric layer, at least partially within the recess of the isolation region and on the exposed portion of the substrate;

(d) forming an electrode layer over the capacitor dielectric layer;

(e) forming a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

(f) forming a doped region within the substrate and adjacent to the pass-gate and the electrode layer.

15. (original) The method of claim 14, wherein the steps (c) and (d) comprise:

after step (b), substantially conformally forming the capacitor dielectric layer over the first dielectric layer;

forming a planarization layer over the electrode layer; and removing portions of the planarization layer, the capacitor dielectric layer and the electrode layer directly over the first dielectric layer.

16. (original) The method of claim 15, wherein the planarization layer is a dielectric layer.

17. (original) The method of claim 15, wherein the planarization layer is a photoresist layer.

18. (original) The method of claim 17 further comprising the step of removing the photoresist layer within the opening of the first dielectric layer after the removing portions step.

19. (original) The method of claim 14, wherein a space between the pass-gate and the exposed portion of the substrate is from about 400Å to about 1500Å.

20. (original) The method of claim 14, wherein the capacitor dielectric layer comprises a high dielectric constant material layer.

21. (original) The method of claim 20, wherein the capacitor dielectric layer is formed by atomic layer deposition (ALD).

22. (original) The method of claim 20, wherein the electrode layer comprises a metal layer.

23. (original) The method of claim 14, wherein the doped region has a dopant concentration lower than that of the S/D region.

24-38. (canceled)

39. A method of forming a one-transistor memory cell, comprising:

(a) forming a dielectric layer over a substrate having a pass gate formed thereon;

(b) forming an opening in the dielectric layer to expose at least a portion of the substrate adjacent to the pass-gate;

(c) conformally forming a capacitor dielectric layer on sidewalls of the opening in the dielectric layer and on the exposed portion of the substrate; and

(d) conformally forming an electrode layer over the capacitor dielectric layer along sidewalls of the opening in the dielectric layer and over the exposed portion of the substrate, leaving a remaining portion of said opening.

40. (new) The method of claim 39, wherein step (b) further comprises the steps of forming a recess in an isolation region within the substrate, and steps (c) and (d) further comprise forming the capacitor dielectric layer and the electrode layer along walls of the recess of the isolation region.

41. (new) The method of claim 39,

wherein portions of the capacitor dielectric layer and electrode layer are formed over a top surface of said dielectric layer, the method further comprising:

forming a planarization layer over the electrode layer and in the remaining portion of said opening; and

removing portions of the planarization layer, the capacitor dielectric layer and the electrode layer over the top surface of said dielectric layer.

42. (new) The method of claim 41, wherein the planarization layer is a dielectric layer.

43. (new) The method of claim 41, wherein the planarization layer is a photoresist layer.

44. (new) The method of claim 43, further comprising the step of removing the photoresist layer within the opening of the dielectric layer after the removing portions step.

45. (new) The method of claim 41, wherein said removing step comprises a CMP process.

46. (new) The method of claim 39, wherein step (b) further comprises using a second dielectric layer formed on a sidewall of the pass-gate as an etching stop layer.

47. (new) The method of claim 39, wherein a space between the pass-gate and the exposed portion of the substrate is from about 400Å to about 1500Å.

48. (new) The method of claim 39, wherein the capacitor dielectric layer comprises a high dielectric constant material layer.

49. (new) The method of claim 48, wherein the capacitor dielectric layer is formed by atomic layer deposition (ALD).

50. (new) The method of claim 48, wherein the electrode layer comprises a metal layer.

51. (new) The method of claim 39 further comprising:

(e) forming a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

(f) forming a doped region within the substrate and adjacent to the pass-gate and the electrode layer.

52. (original) The method of claim 51, wherein the doped region has a dopant concentration lower than that of the S/D region.